8086 ARCHITECTURE

RISK ASSESSMENT: *Low*

SAFETY CONSIDERATIONS:

Electrical Shock Hazard

Electrostatic Discharge

ENVIRONMENTAL CONSIDERATIONS:

None

TERMINAL LEARNING OBJECTIVE

ACTION: Communicate how an 8086 microprocessor functions.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, and official OMEMS reference material.

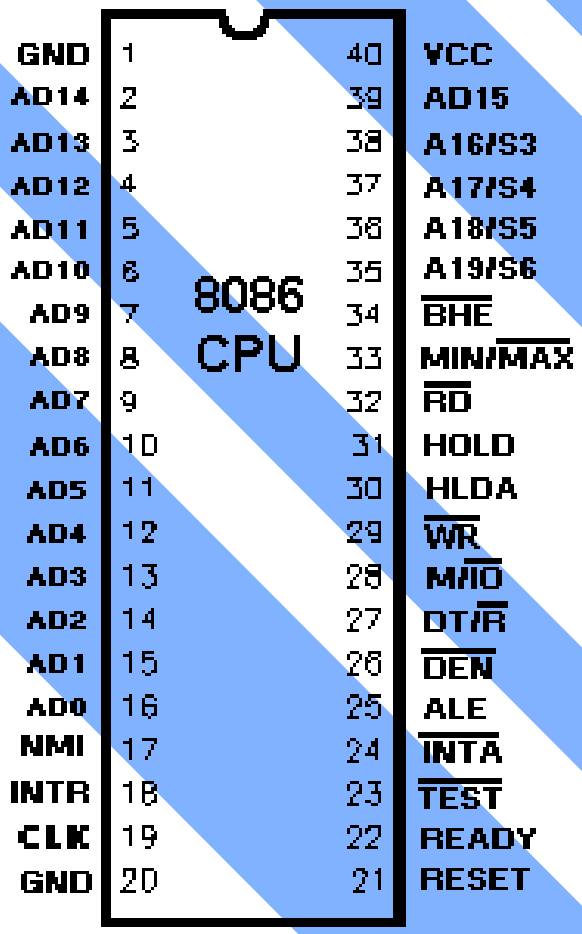
STANDARDS: Correctly answer 18 of 25 questions on how an 8086 microprocessor functions.

ENABLING LEARNING OBJECTIVE

ACTION: Describe the minimum/maximum mode of the 8086 microprocessor.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, and official OMEMS reference material.

STANDARDS: Correctly answer 18 of 25 questions on how an 8086 microprocessor functions.



A17	A16	SEG REG
0	0	ES
0	1	SS
1	0	CS
1	1	DS

8086 MICROPROCESSOR PIN-OUT

MINIMUM MODE

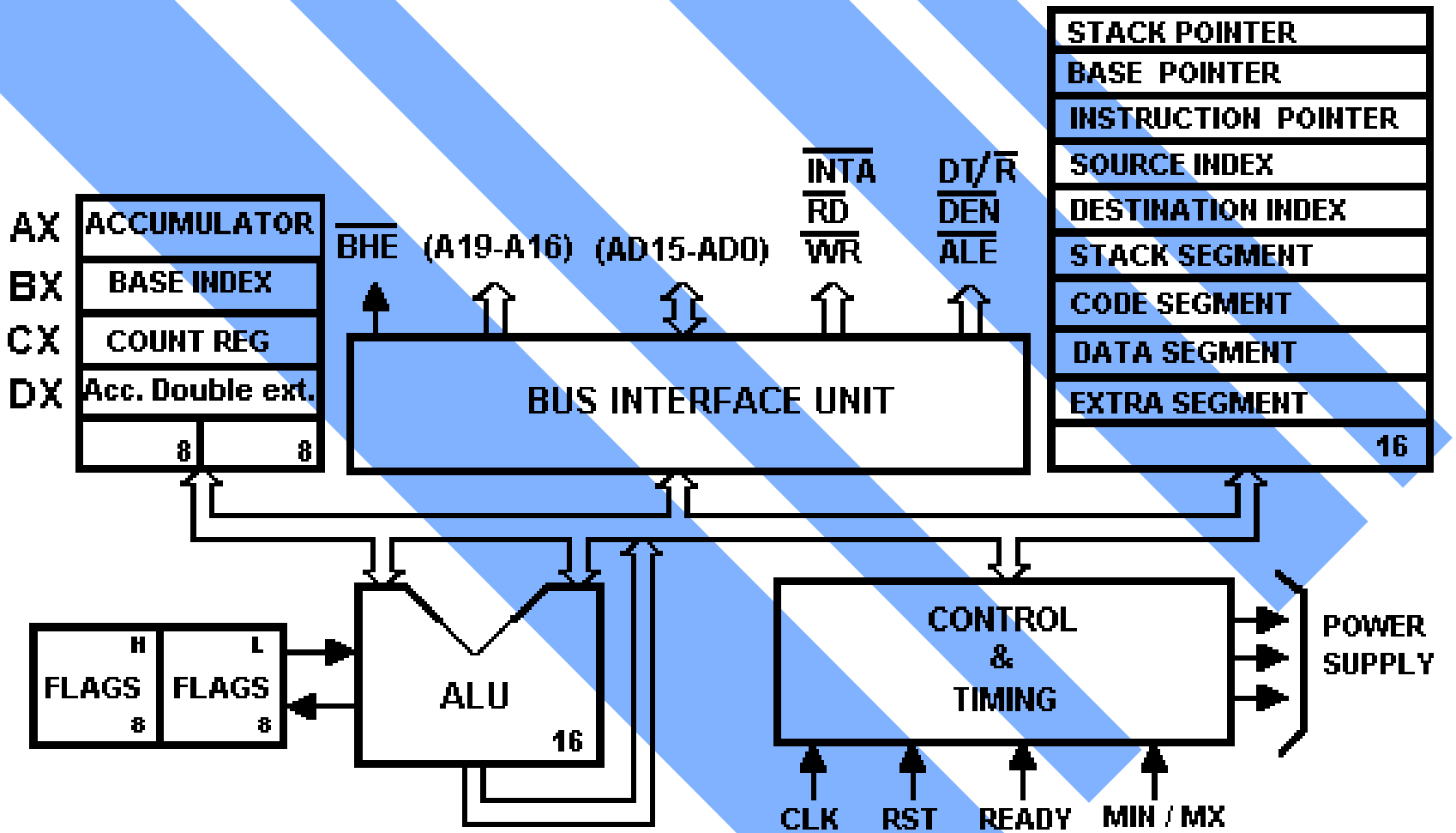
CF351K02-0

ENABLING LEARNING OBJECTIVE

ACTION: Describe the purpose of the Control, ALU, Internal Registers and Buses of the 8086 Microprocessor.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, and official OMEMS reference material.

STANDARDS: Correctly answer 18 of 25 questions on how an 8086 microprocessor functions.



8086 BLOCK DIAGRAM

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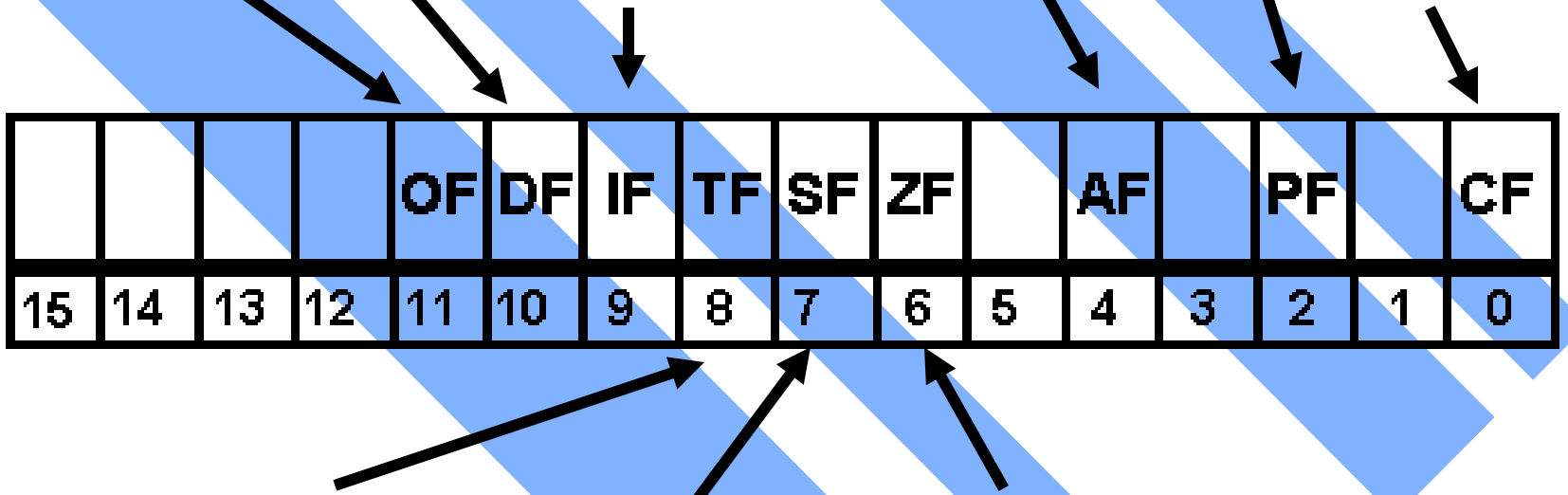


8086 FLAG REGISTER

GENERAL PURPOSE REGISTERS

HIGH BYTE	GP REGISTERS	LOW BYTE
AH	AX	AL
BH	BX	BL
CH	CX	CL
DH	DX	DL

8 BIT **16 BIT**

8086 POINTER/SEGMENT/INDEX REGISTERS

POINTERS	**SEGMENTS**	**INDEX**
INSTRUCTION POINTER	CODE SEGEMENT	SOURCE
STACK POINTER	STACK SEGMENT	DESTINATION
BASE POINTER	DATA SEGMENT	
	EXTRA SEGMENT	

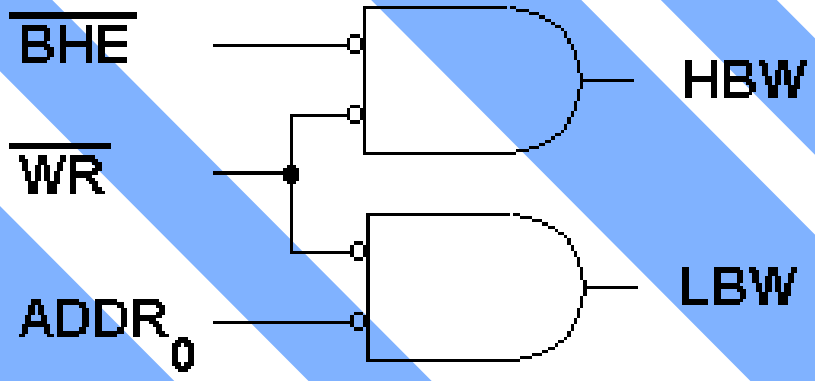
ENABLING LEARNING OBJECTIVE

ACTION: Define memory and I/O operation on a multiplexed bus.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, and official OMEMS reference material.

STANDARDS: Correctly answer 18 of 25 questions on how an 8086 microprocessor functions.

BHE
ADD0
FFFF
FFFD
FFFB
HIGH BANK
ODD
FFFE
FFFC
FFFA
LOW BANK
EVEN
0005
0003
0004
0002
D15 D8
D7 D0

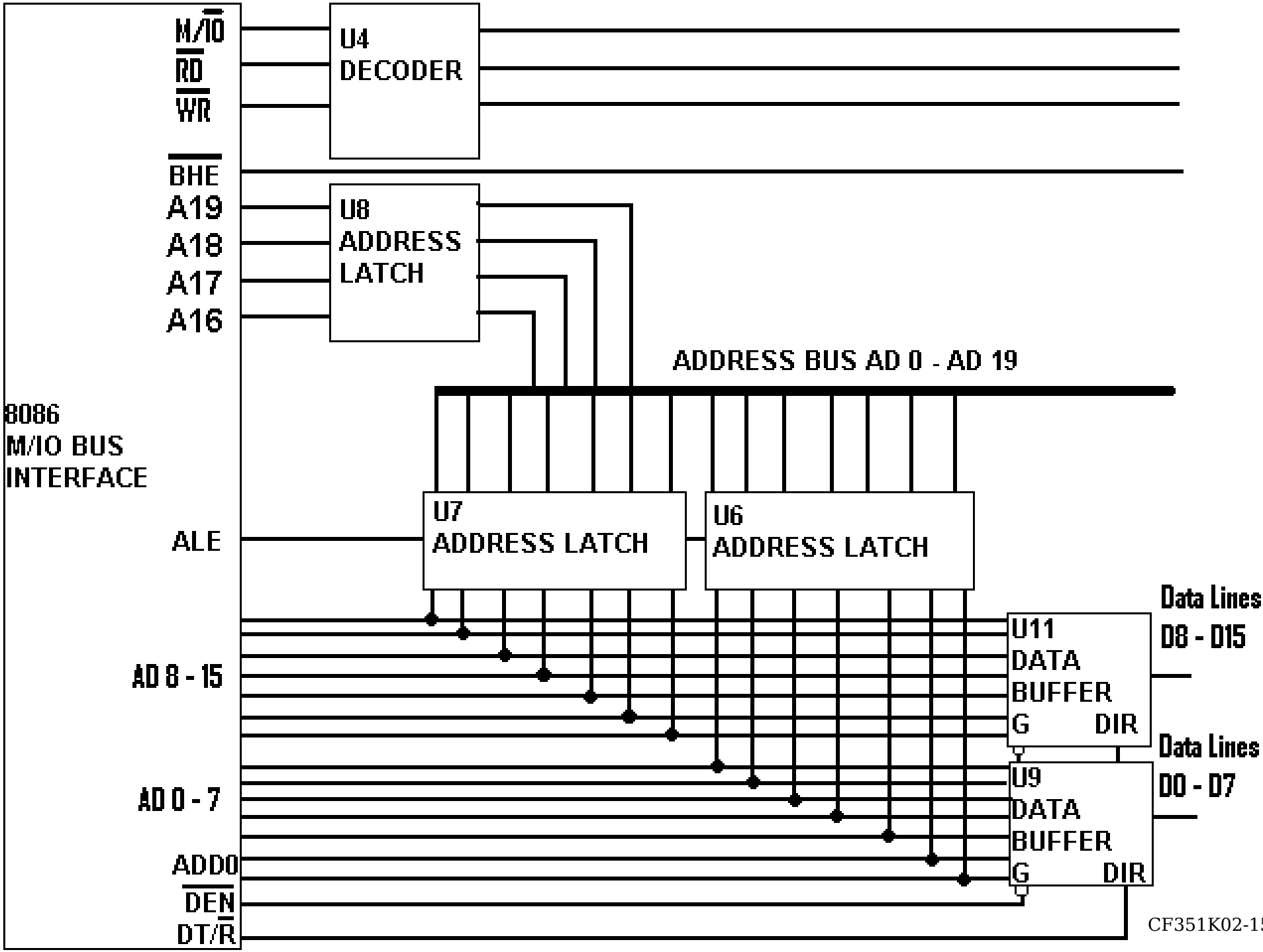


$\overline{BHE}$	$ADDR_0$	FUNCTION
0	0	16-BIT transfer both banks
0	1	8-BIT transfer high bank
1	0	8-BIT transfer low bank
1	1	NO bank transfer

MEMORY WRITE BANK SELECTION

MEMORY READ BANK SELECTION

- During a read 16-bits are always transferred. The 8086 microprocessor uses the data it needs (low byte, high byte, word) without any conflicts or problems.


M/IO
RD
WR
BHE
A19
A18
A17
A16
U4
DECODER
U8
ADDRESS
LATCH
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
AD 0 - 7
ADD0
DEN
DT/R

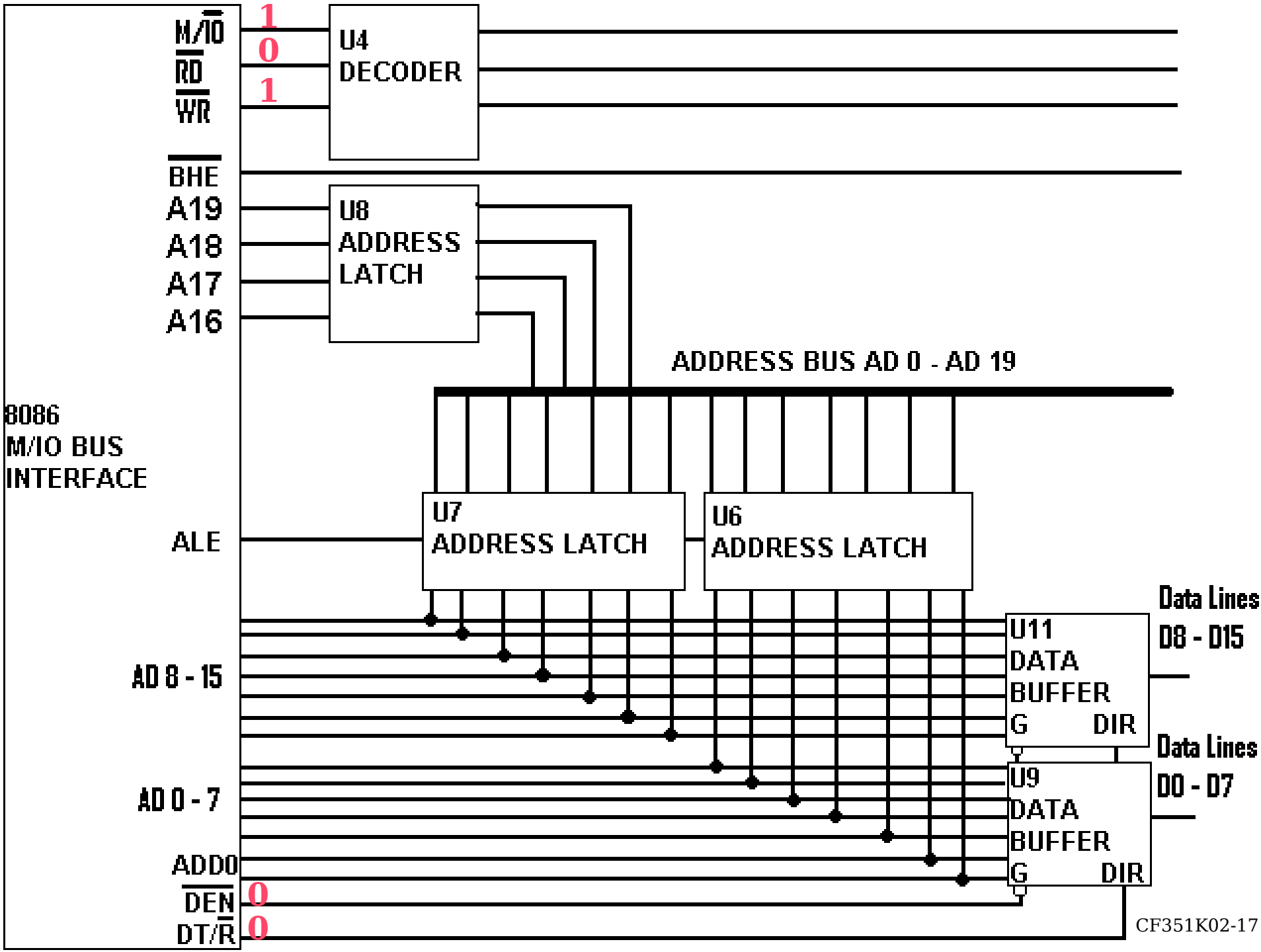
CF351K02-15

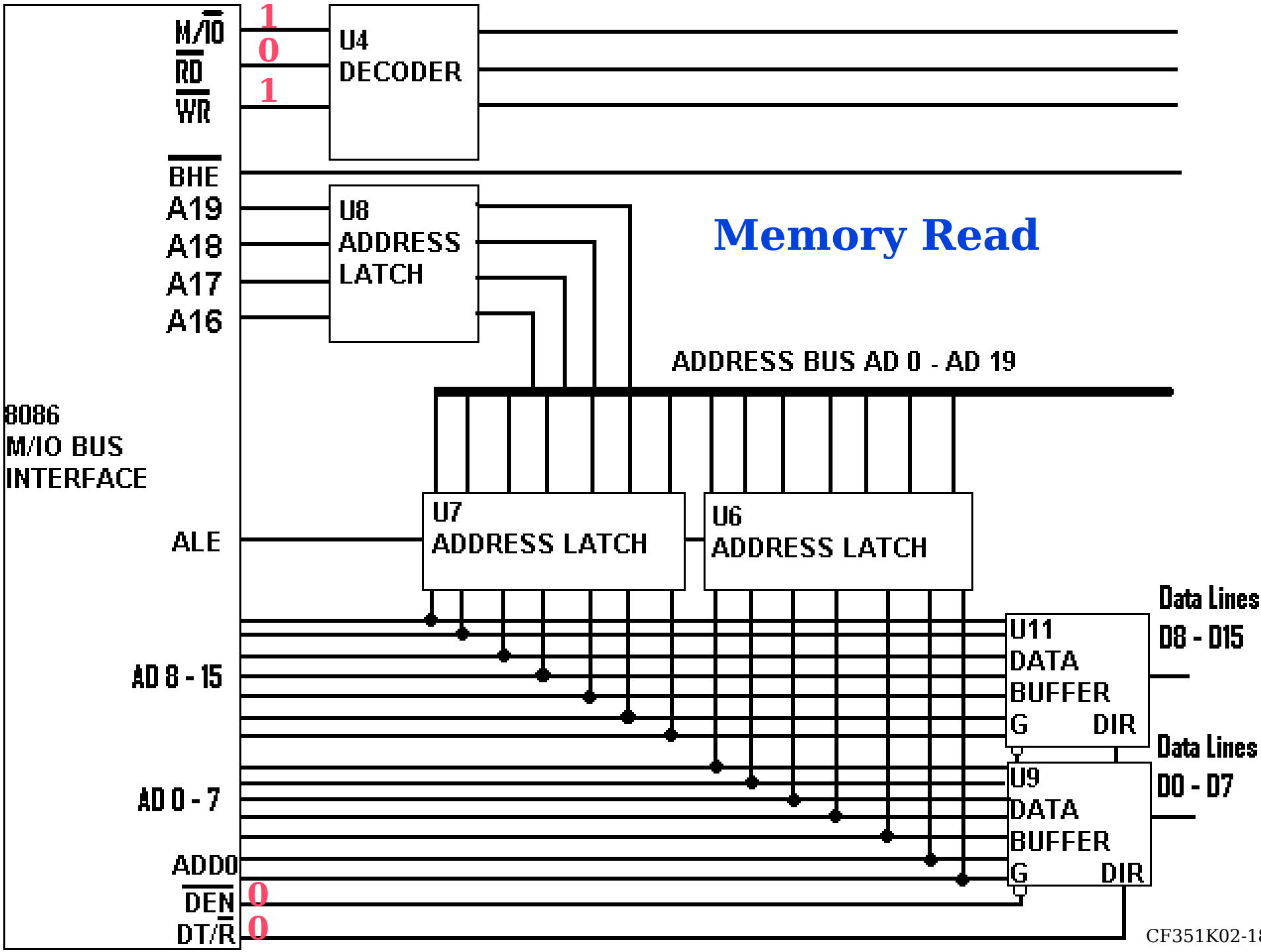
ENABLING LEARNING OBJECTIVE

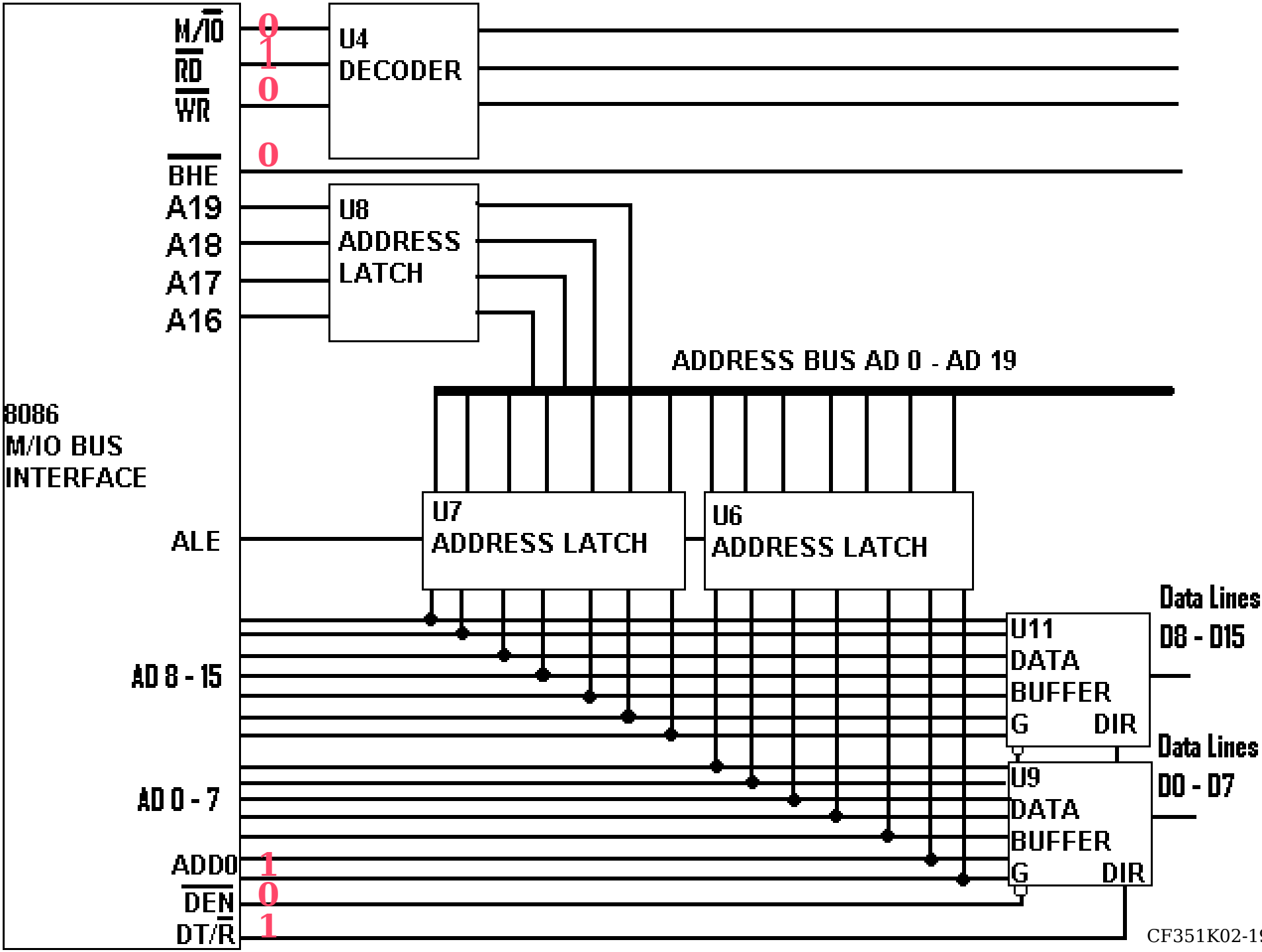
ACTION: Define the architecture of the 8086 Microprocessor.

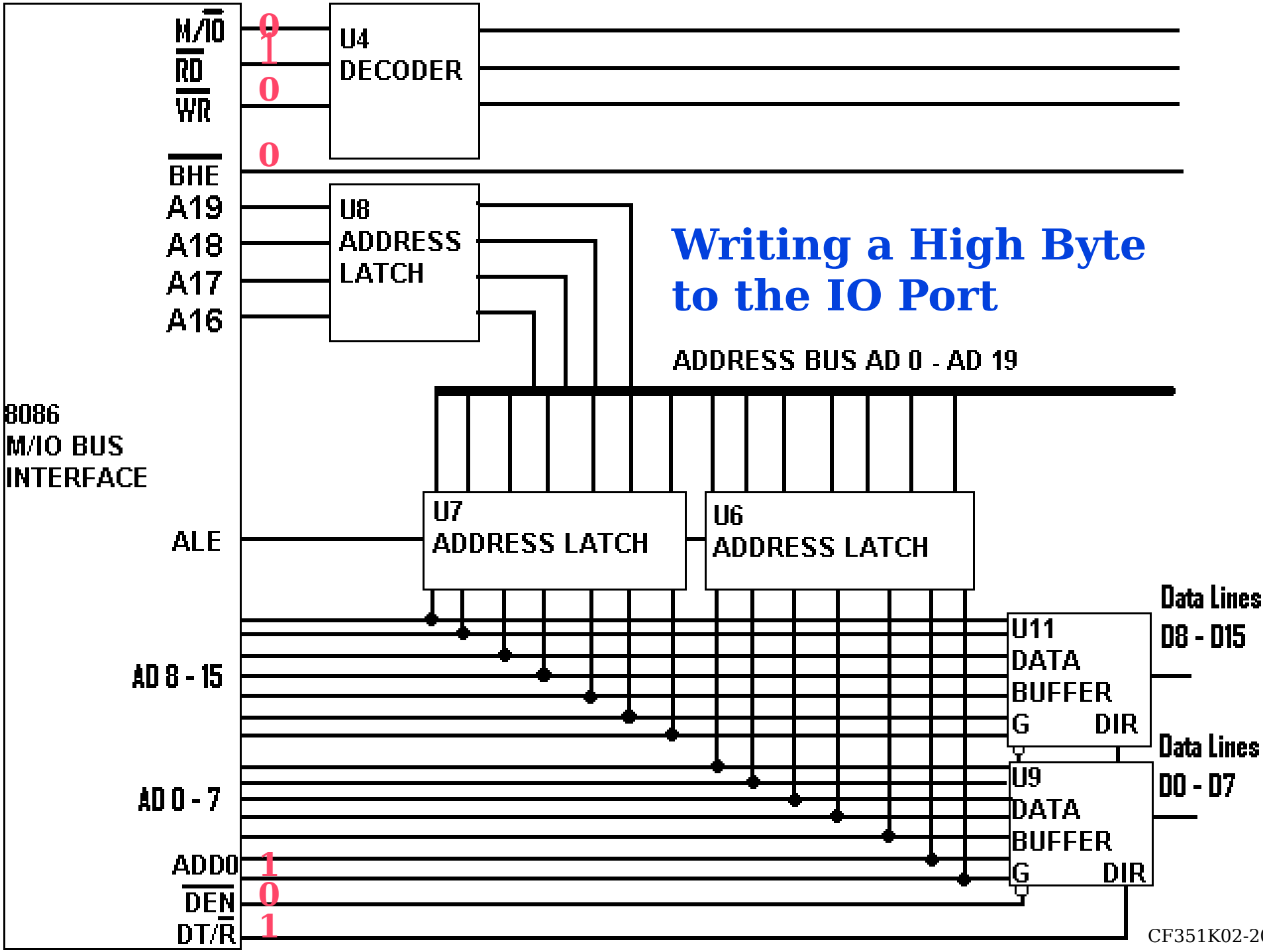
CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, and official OMEMS reference material.

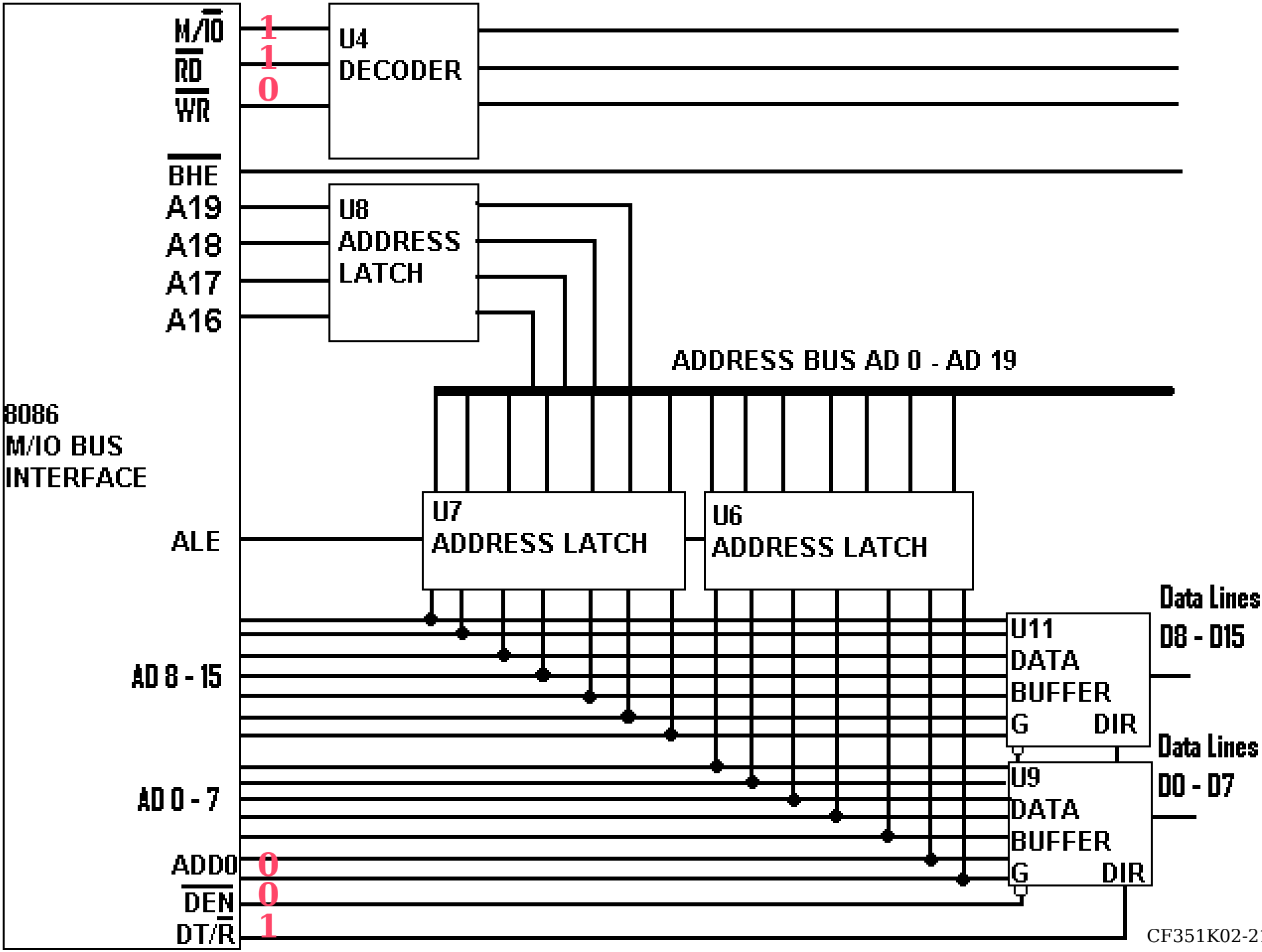
STANDARDS: Correctly answer 18 of 25 questions on how an 8086 microprocessor functions.


M/IO
RD
WR
1
0
1
U4
DECODER
BHE
A19
A18
A17
A16
U8
ADDRESS
LATCH
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
AD 0 - 7
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
ADD0
DEN
0
DT/R
0
CF351K02-17

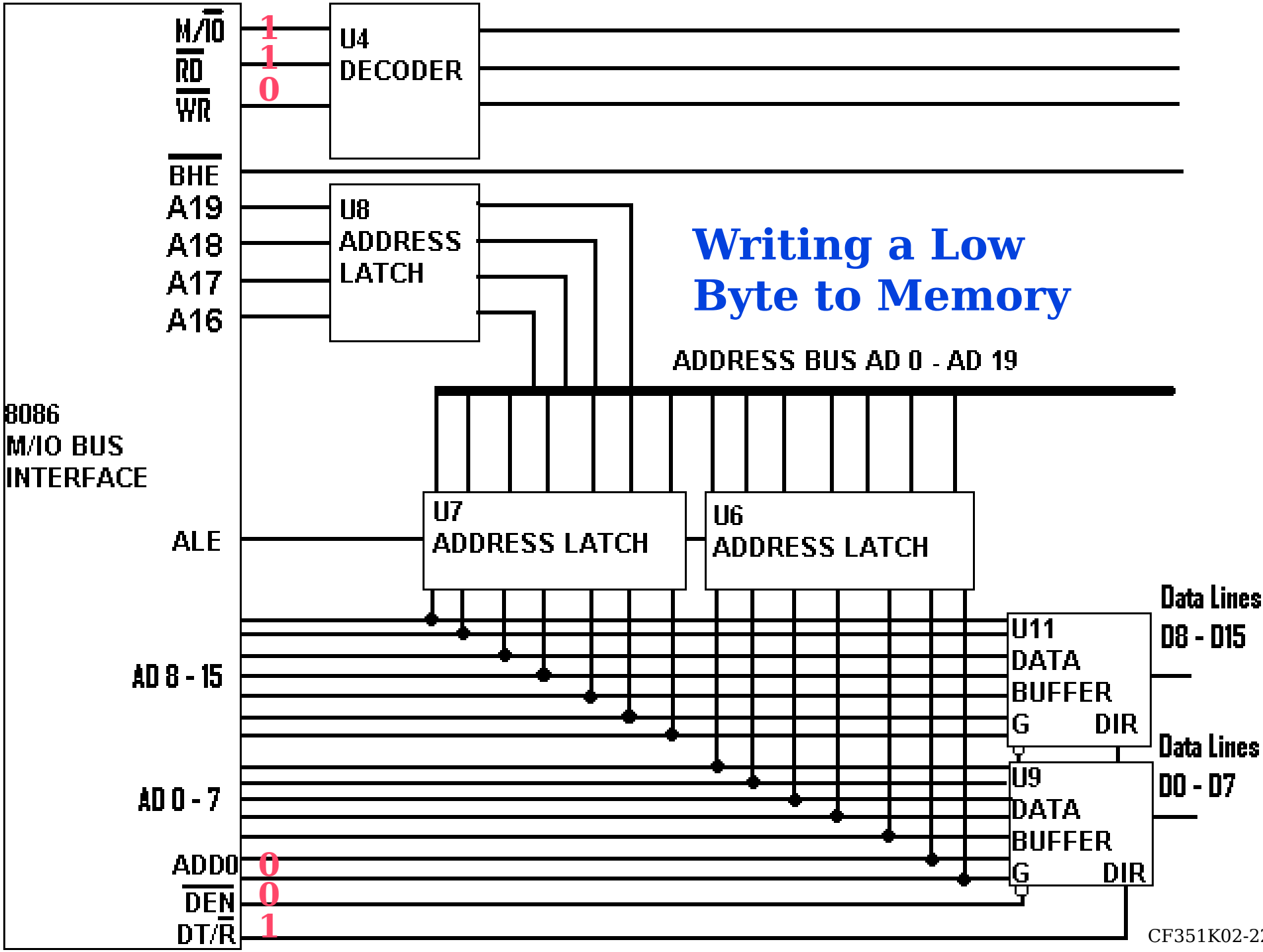

M/IO
RD
WR
1
0
1
U4
DECODER
BHE
A19
A18
A17
A16
U8
ADDRESS
LATCH
Memory Read
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
AD 0 - 7
ADD0
DEN
0
DT/R
0
CF351K02-18


M/IO
RD
WR
BHE
A19
A18
A17
A16
0
1
0
0
U4
DECODER
U8
ADDRESS
LATCH
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
AD 8 - 15
AD 0 - 7
ADDO
DEN
DT/R
1
0
1
U11
DATA
BUFFER
G
DIR
U9
DATA
BUFFER
G
DIR
Data Lines
D8 - D15
Data Lines
D0 - D7
CF351K02-19


M/IO
RD
WR
BHE
A19
A18
A17
A16
0
1
0
0
U4
DECODER
U8
ADDRESS
LATCH
Writing a High Byte
to the IO Port
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
AD 0 - 7
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
ADD0
DEN
DT/R
1
0
1


M/IO
RD
WR
1
1
0
U4
DECODER
BHE
A19
A18
A17
A16
U8
ADDRESS
LATCH
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
AD 0 - 7
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
ADD0
0
DEN
0
DT/R
1

CF351K02-21


M/IO
RD
WR
1
1
0
U4
DECODER
BHE
A19
A18
A17
A16
U8
ADDRESS
LATCH
Writing a Low
Byte to Memory
ADDRESS BUS AD 0 - AD 19
8086
M/IO BUS
INTERFACE
ALE
U7
ADDRESS LATCH
U6
ADDRESS LATCH
Data Lines
D8 - D15
U11
DATA
BUFFER
G
DIR
AD 8 - 15
AD 0 - 7
Data Lines
D0 - D7
U9
DATA
BUFFER
G
DIR
ADD0
0
DEN
0
DT/R
1
CF351K02-22